

## Numerical Simulation of Thermal Conductivity in Silicon Wafers of Transistors

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**Abstract.** This article presents studies of thermal conductivity in silicon wafers of microcontroller transistors and electronic devices. The focus is on modeling the thermal conductivity of silicon wafers to analyze temperature field distribution under different operating modes and thermal loads. Heat propagation in solids is described by the three-dimensional Fourier equation of thermal conductivity. Methods are applied to solve differential equations considering geometric and physical parameters of the material. The algorithm is based on an analytical–numerical method for decomposing the temperature field into a polynomial series. The modeling results allow evaluation of the effect of transistor miniaturization on thermal characteristics and propose approaches to optimizing heat dissipation. The practical significance lies in improving reliability and energy efficiency of modern microcontrollers. The results show how quickly heat propagates in transistors, calculated using the recurrent-operator method. Simulation in Maple demonstrates that peak temperature gradients are localized in central crystal regions, where the sine function reaches maximum, and decay exponentially toward edges. This computational algorithm can be integrated into microcontroller memory subsystems, where transistors are densely packed, for predictive throttling—automatic reduction of recording frequency in the event of local overheating threats.

**Keywords:** thermal conductivity, modeling, transistors, mosfets.

### Introduction

Modern computing systems are based on the use of transistors, which are characterized by low cost, compact size and high reliability. However, with the miniaturization and increasing integration density of transistors, the issue of thermal conductivity of the materials from which they are made becomes increasingly important. Thermal conductivity is a molecular transfer of heat in a continuous medium and depends on the state of aggregation of a substance, its composition, purity, temperature and pressure. This property is critically important for transistors, since the uneven temperature distribution in semiconductor structures leads to local overheating, changes in performance, and reduced reliability. In addition, thermal conductivity can change under the influence of external factors — pressure, magnetic field, radiation - as well as due to structural changes in the material (heat treatment, wear). In translucent media used in a number of semiconductor technologies, thermal conductivity is accompanied by radiative energy transfer, which complicates heat transfer processes. Thus, the study of thermal conductivity in transistors is of key importance for improving the efficiency of modern computing systems, since their stability and durability depend on the ability of materials to effectively remove heat.

The objectives of the study of this topic are:

- identify patterns of distribution of heat fluxes in silicon and silicon carbide substrates.
- construct an analytic-numerical approximation of the three-dimensional Fourier equation to describe the temperature modes of transistors.
- evaluate the efficiency of heat dissipation in silicon and 4H-SiC, identify advantages and disadvantages for use in microcontrollers.
- create a tool to predict thermal conditions and prevent transistor degradation at high integration density.

To achieve this goal, the following research tasks follow:

- build a mathematical model of heat propagation in transistor structures using Maple.
- implement an algorithm for decomposing a temperature field into a polynomial series.
- perform thermal conductivity modeling for silicon and silicon carbide substrates.
- visualize the temperature distribution in the form of three-dimensional graphs.
- compare simulation results for different materials and draw conclusions on thermal stability.

The practical significance of this study is:

- the model can be integrated into the memory subsystems of microcontrollers to automatically reduce the recording frequency in case of overheating.

- using the model allows you to take into account thermal limitations in advance and avoid degradation of transistors.
- results show that the use of SiC significantly accelerates the relaxation of thermal energy, which makes it promising for high-performance systems.
- the study makes it possible to create more durable and stable computing systems due to efficient heat dissipation.

The development of semiconductor technologies is based on fundamental research initiated in the middle of the 20th century by W. Shockley on the theory of semiconductors and the development of MOSFET structures [1,2]. In modern conditions, as B. Rayner notes, thermal management in microelectronics is becoming a critical factor due to the extreme density of component integration. According to the reviews [3], for Internet of Things (IoT) systems, energy efficiency and reliability issues directly depend on the ability of materials to efficiently distribute and dissipate heat in pulsed modes of operation. The use of modern STM32G4 or nRF52840 series microcontrollers requires a detailed understanding of thermal processes at the crystal level to prevent their degradation. The transistor is an electronic switch with two states - "on" and "off", which is controlled by applying voltage or current to the control electrode[4]. There are two main classes of transistors: bipolar (bipolar junction transistors, BJT) and MOSFET transistors - metal oxide semiconductor field effect transistors (MOSFET), which are also often called field effect transistors[5]. After more than thirty years of rapid development of semiconductor technologies, engineers have been able to place about one billion MOSFETs on one square centimeter of a silicon crystal[6]. At the same time, the cost of each transistor is less than ten cents. Over time, the integration density of transistors on a chip increases approximately tenfold every eight years, and the cost of one element decreases [7].

Today, MOSFETs act as the fundamental "building blocks" from which almost all digital systems are formed. MOSFETs are made on the basis of silicon, an element widely used in rocks and sand. Silicon (Si) belongs to group IV of the periodic table and has four valence electrons [8]. Due to this, it is able to form bonds with four neighboring atoms, forming an ordered crystal lattice. In Figure 1 (a), for clarity, the lattice is represented in a two-dimensional coordinate system, but in reality its structure has a cubic shape. The lines in the figure indicate covalent bonds between atoms. By its nature, silicon is a weak conductor, since its electrons are fully involved in the formation of covalent bonds. However, the electrical properties of silicon can be significantly improved by introducing a small number of impurity atoms (dopant)[9]. If a group V element, such as arsenic (As), is used as an impurity, then each impurity atom contains an additional electron that is not involved in the formation of covalent bonds. This free electron is able to move easily inside the crystal lattice. In this case, the arsenic atom, which has lost an electron, turns into a positively charged ion ( $\text{As}^+$ )[10], as shown in Fig. 1(b).

The electron has a negative charge, therefore arsenic is classified as an impurity of type n (n type dopant). In the case of using a group III element, such as boron (B), one electron is missing from each impurity atom, as shown in Figure 1 (c). This missing electron is called a "hole". An electron from a neighboring silicon atom can pass to a boron atom and fill in the missing bond. As a result, the boron atom, which has received an additional electron, becomes a negative ion ( $\text{B}^-$ ), and a hole forms in the silicon atom. Thus, the hole is able to move through the crystal lattice in the same way as an electron[11]. Despite the fact that a hole represents only the absence of a negative charge, in a semiconductor it behaves like a positively charged particle. That is why boron is classified as a p-type dopant. Since the conductivity of silicon can vary by orders of magnitude depending on the concentration of impurities, this material is classified as a semiconductor[12]

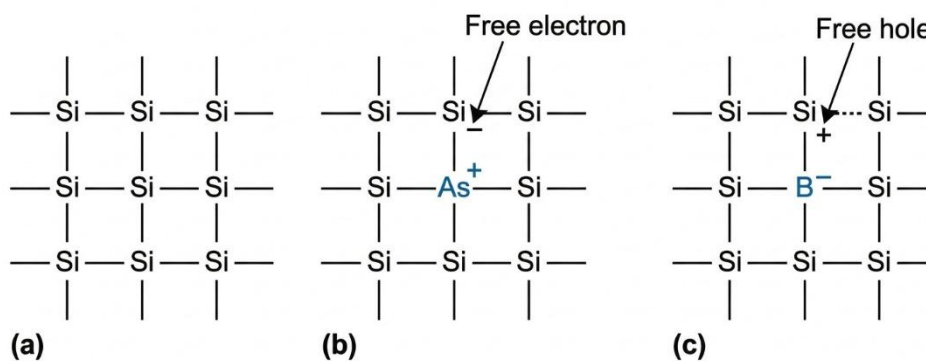


Fig.1. – Silicon lattice and impurity atoms

The electrical conductivity of a semiconductor material is determined by its crystal structure, the concentration of charge carriers, and temperature conditions[13]. The basis of most modern electronic devices is monocrystalline silicon, the atoms of which form a stable tetrahedral lattice with four covalent bonds. The energy of one such bond is about 1.12 eV, which corresponds to the band gap silicon at a temperature of 300 K. In the pure (intrinsic) state, silicon has extremely low conductivity, on the order of  $4.4 \times 10^{-4}$  Cm/m, at room temperature. This is due to the fact that at 300 K the concentration of free charge carriers (electrons and holes) is only  $1.5 \times 10^{10} \text{ cm}^{-3}$ , which is many orders of magnitude less than in metals, where the number of carriers reaches  $10^{22} \text{ cm}^{-3}$ . As the temperature increases, thermal excitation of electrons occurs, which pass from the valence band to the conduction band, forming electron-hole pairs[14]. The concentration of such pairs increases exponentially with increasing temperature in accordance with the law[15] :

$$n_i = \sqrt{N_c \cdot N_v} \cdot e^{-\frac{E_g}{2kT}} \quad (1)$$

where  $n_i$  - the concentration of carriers (electrons and holes) in the intrinsic state,

$E_g$  - the band gap,

$k$  - the Boltzmann constant,

$T$  - the temperature (in Kelvin). The concentration of electrons in the conduction band

$N_c$  - the effective density of states in the conduction band.,

$N_v$  - the effective density of states in the valence band,

$E_g$  - the width of the forbidden zone,

The concentration of electrons in the conduction band

$$n = N_c e^{\frac{E_c - E_F}{kT}} \quad (2)$$

The concentration of electrons in the conduction band:

$$p = N_v e^{\frac{E_F - E_v}{kT}}; \quad (3)$$

In an intriguing case:

$$n = p = n_i \quad (4)$$

| Material     | Density (g/sm <sup>3</sup> ) | Band gap width (eV) | Thermal Conductivity (W/m*K) |
|--------------|------------------------------|---------------------|------------------------------|
| Silicon (Si) | 2.33                         | 1.12                | 150                          |

The relationship between the above formulas (1-4) and the thermophysical properties of the material lies in the direct dependence of the concentration of charge carriers on temperature conditions. Formula (1) shows that the intrinsic concentration of  $n_i$  increases exponentially with increasing absolute temperature  $T$ . This leads to a corresponding change in the concentration of electrons (2) and holes (3) in the conduction and valence bands. The choice of silicon as the main material is due to its ability to maintain stability under such changes: having a high thermal conductivity (150 W/m·K), it provides efficient heat dissipation generated by thermal excitation of carriers[16]. Unlike germanium or gallium arsenide, silicon provides an optimal balance between carrier mobility and thermal stability, which minimizes local overheating described by these mathematical relationships. Thus, the formulas describe the electrical state of the system, which directly dictates the requirements for thermal conductivity studied in this work.

Silicon has an optimal set of characteristics: relatively low density, which facilitates crystal processing, and high thermal conductivity, which ensures efficient heat removal from the active elements of the microcircuits. Denser materials, such as germanium or gallium arsenide (GaAs), exhibit significantly greater carrier mobility — up to 8,500 cm<sup>2</sup>/(V·s) for electrons in GaAs versus 1,400 cm<sup>2</sup>/(V·s) in silicon. However, they are inferior to silicon in terms of thermal stability and create additional difficulties in mass production[17].

**Research methods.** To study the temperature conditions of the microcontroller crystal, a mathematical model was developed in the symbolic computing environment of Maple. The propagation of heat in a solid is described by the three-dimensional Fourier differential equation of thermal conductivity. The algorithm is based on an analytical numerical method for decomposing the temperature field into a polynomial series. The program defines the following parameters of the studied area and material properties: thermal conductivity coefficients along the  $x$ ,  $y$  and  $z$  axes:

For Si  $a = 0.000028 \text{ m}^2/\text{s}$ .

For 4H-SiC  $\alpha = 0.43 \text{ m}^2/\text{s}$  (at a temperature of 300K).

Geometric dimensions of the crystal (or the fragment under study):

A harmonic function with exponential decay in time is chosen as the basic (initial) function of the space-time distribution  $g(x, y, z, t)$ :

$$g = \sin\left(\frac{\pi x}{l_1}\right) \sin\left(\frac{\pi y}{l_2}\right) \sin\left(\frac{\pi z}{l_3}\right) e^{-t} \quad (5)$$

To construct the approximating polynomial  $q$ , the algorithm uses the recursive procedure  $Q(i, j, k, p)$ , which calculates the weighting coefficients for the terms of the series based on the thermal conductivity coefficients. The logic of the function is such that if the indexes are negative, 0 is returned, the base point (0,0,0,0) is 1, and the subsequent ones are calculated as:

$$Q(i, j, k, p) = -Q(i, j-2, k, p) - Q(i, j, k-2, p) + \alpha Q(i-1, j, k, p-1) \quad (6)$$

Next, the program calculates the partial derivatives of the basic function  $g$  in terms of spatial coordinates and time using the  $fd(j, k, p)$  procedure. The final temperature distribution function  $q$  is formed as the sum of the terms of the series (the code uses nested summation cycles from 0 to 2 for each variable):

$$q = \sum_{i=0}^2 \sum_{j=0}^2 \sum_{k=0}^2 \sum_{p=0}^2 Q(i, j, k, p) \frac{x^{i+j+k+p}}{(i+j+k+p)!} fd(j, k, p) \quad (7)$$

This approach makes it possible to obtain a highly accurate analytical approximation of the temperature field inside the transistor structure under specified boundary conditions.

**Simulation results.** Based on the constructed polynomial  $q$ , graphs of three-dimensional surfaces visualizing the temperature distribution were generated in the Maple environment. For modeling and analysis, a transistor was selected along the  $x=0.02\text{m}$ ,  $y=0.01\text{m}$ ,  $z=0.005\text{m}$  axes, and a slice along the application axis  $z = 0.003 \text{ m}$  was also selected at time  $t = 0.1\text{s}$ .

The command `plot3d(q, x=0..l1, y=0..l2)` generates a surface where the  $x$  and  $y$  axes correspond to the geometric dimensions of the chip (from 0 to 0.02 and from 0 to 0.01, respectively), and the vertical axis displays the temperature value. Table 1 shows the results of calculations of the thermal conductivity of a silicon wafer at arbitrary values of axes and time, taking into account the set limits. We considered the process in a parallelepiped of volume  $V = l_1 \cdot l_2 \cdot l_3$ ; The process was considered within the initial and boundary conditions.

$$q(x, y, z, t)_{x=0, l_1; 0 < x < l_1, 0 < y < l_2, 0 < z < l_3;}$$

**Table 1.** Simulation results of thermal conductivity of a silicon wafer

| $t, \text{s}$ | $x, \text{m}$ | $y, \text{m}$ | $z, \text{m}$ | $q, \text{m/s}^2$           |
|---------------|---------------|---------------|---------------|-----------------------------|
| 0.01          | 0.01          | 0.01          | 0.003         | $9.051753714 \cdot 10^{-6}$ |
| 0.05          | 0.003         | 0.003         | 0.003         | $7.939668209 \cdot 10^{-7}$ |
| 0.1           | 0.001         | 0.001         | 0.001         | $2.800843856 \cdot 10^{-8}$ |
| 1             | 0.02          | 0.01          | 0.005         | $1.076220762 \cdot 10^{-5}$ |

The results of modeling the thermal conductivity of a silicon substrate (Figures 1-6).

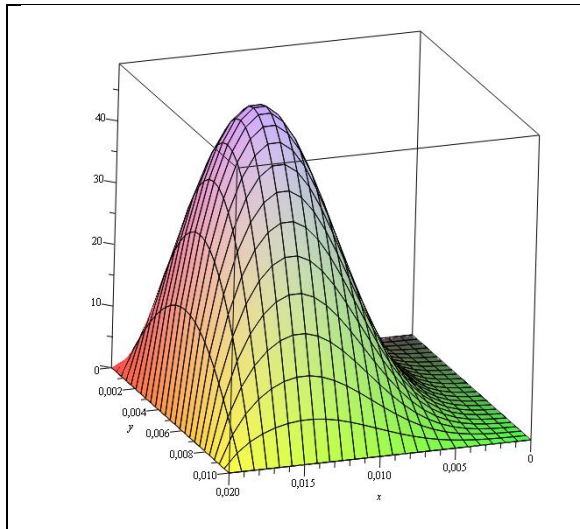


**Fig.1.** - Simulation of thermal conductivity at  $t=0.01s$ ,  $z=0.003m$ , at  $x=0$  to  $0.02$ ,  $y=0$  to  $0.01$

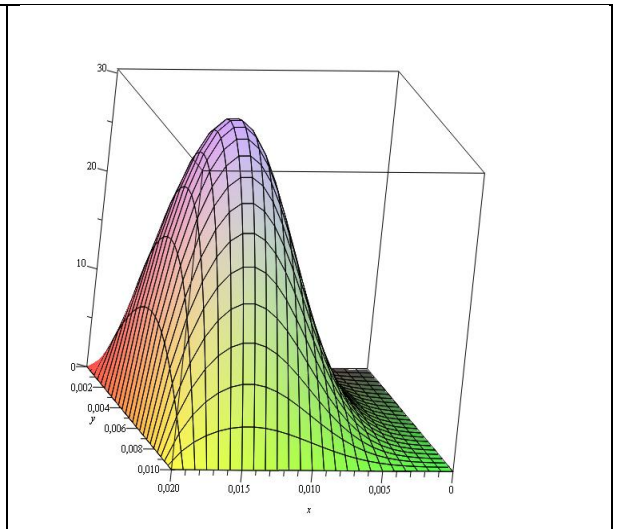


**Fig.2.** - Simulation of thermal conductivity at  $t=0.1s$ ,  $z=0.004m$ , at  $x=0$  to  $0.02$ ,  $y=0$  to  $0.01$

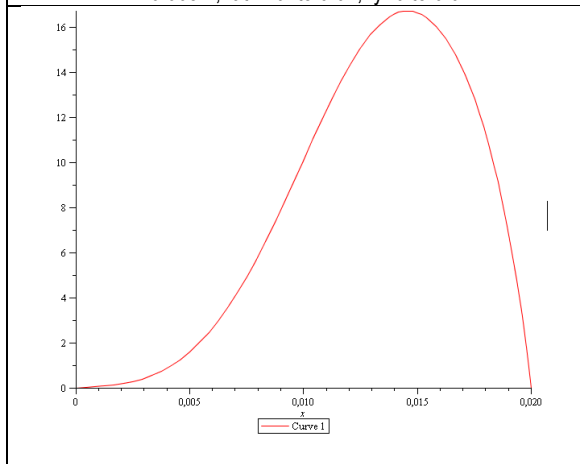


**Fig.3.** - Simulation of the thermal conductivity process along the  $ox$  axis from  $0$  to  $0.02$ , in the section at  $t=0.01s$ ,  $y=0.001m$ ,  $z=0.003m$

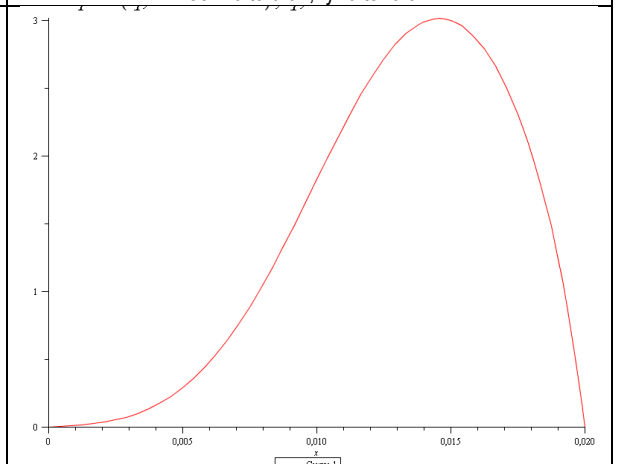


**Fig. 4.** - Simulation of the thermal conductivity process along the  $oy$  axis from  $0$  to  $0.02$  in the section at  $t=0.1s$ ,  $y=0.001m$ ,  $z=0.003m$ .

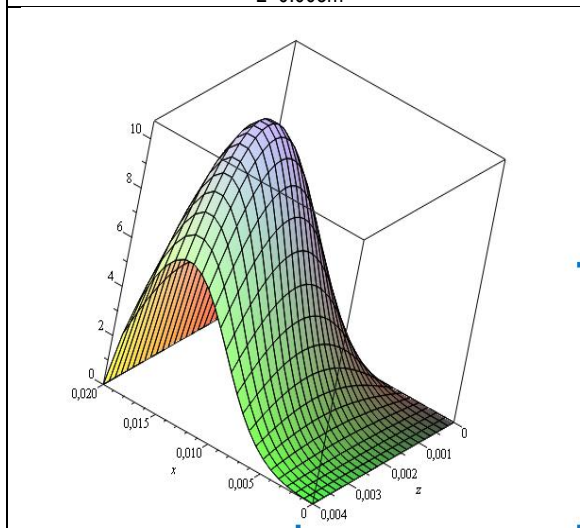


**Fig. 5.** - Simulation of thermal conductivity at  $t=0.5s$ ,  $z=0.003m$  at  $x=0$  to  $0.02m$ ,  $y=0$  to  $0.01$

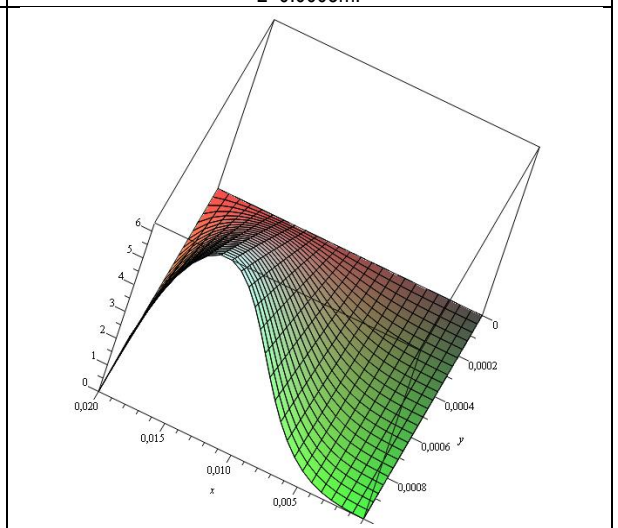


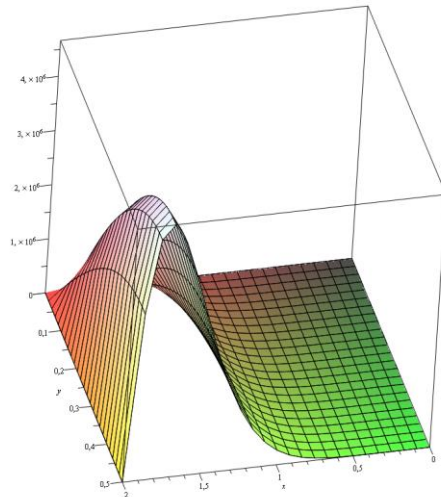
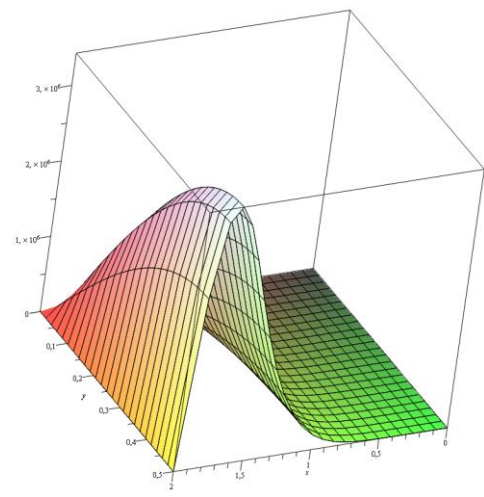
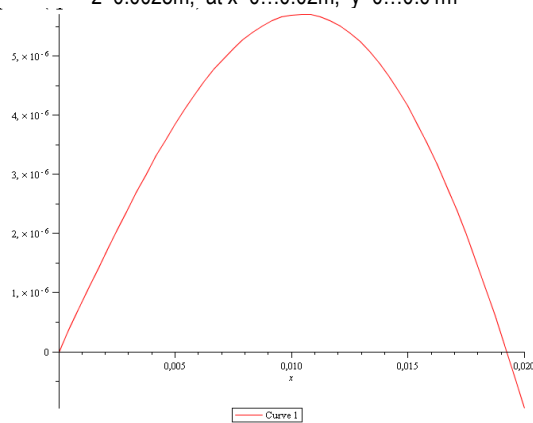
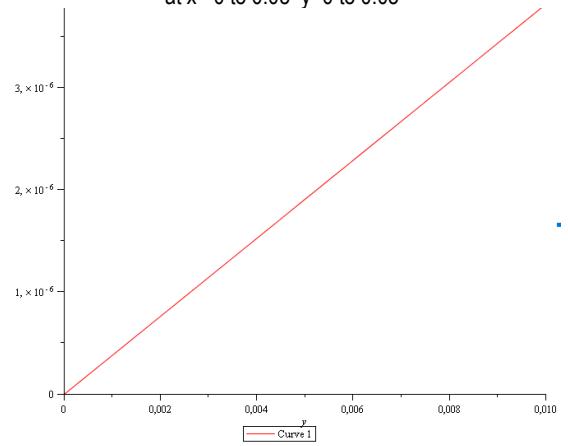
**Fig. 6.** - Simulation of thermal conductivity at  $t=0.5s$ ,  $z=0.001m$ , at  $x=0$  to  $0.02$ ,  $y=0$  to  $0.001$

$$q(x, y, z, t)_{x=0, l_1}; 0 < x < l_1, 0 < y < l_2, 0 < z < l_3;$$

**Table 2.** Simulation results of the thermal conductivity of a silicon carbide wafer at arbitrary values of axes and time

| $t, ms$ | $x, m$ | $y, m$ | $z, m$ | $q \text{ m/s}^2$           |
|---------|--------|--------|--------|-----------------------------|
| 0.01    | 0.01   | 0.005  | 0.0025 | $2.594225522 \cdot 10^{-6}$ |
| 0.05    | 0.003  | 0.003  | 0.003  | $7.706956453 \cdot 10^{-7}$ |
| 0.1     | 0.01   | 0.005  | 0.003  | $2.845080897 \cdot 10^{-6}$ |
| 0.1     | 0.02   | 0.01   | 0.005  | 0                           |

Results of modeling the thermal conductivity of a silicon carbide substrate (Figures 5-8):


**Fig. 7.** - Simulation of thermal conductivity at  $t=0.01s$ ,  $z=0.0025m$ , at  $x=0 \dots 0.02m$ ,  $y=0 \dots 0.01m$ 

**Fig 8.** - Simulation of thermal conductivity at  $t=0.5s$ ,  $z=0.003m$ , at  $x=0$  to  $0.05$   $y=0$  to  $0.05$ 

**Fig. 9.** - Simulation of the heat transfer process in a section along the coordinate axis  $ox$ ,  $x=0$  to  $0.02m$ , at  $t=0.01s$ ,  $z=0.003m$ ,  $y=0.01m$ .

**Fig. 10.** - Simulation of the thermal conductivity process in a slice along the coordinate axis  $oy$ , at  $t=0.5s$ ,  $z=0.003m$ ,  $x=0.01m$ .  $y=0$  to  $0.01$

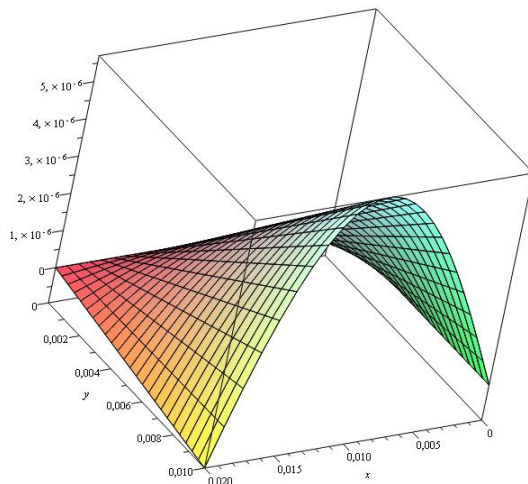


Fig 11. - Simulation of thermal conductivity at  $t=0.5s$ ,  $z=0.33\mu m$  at  $x=3.1$   $y=0.31$

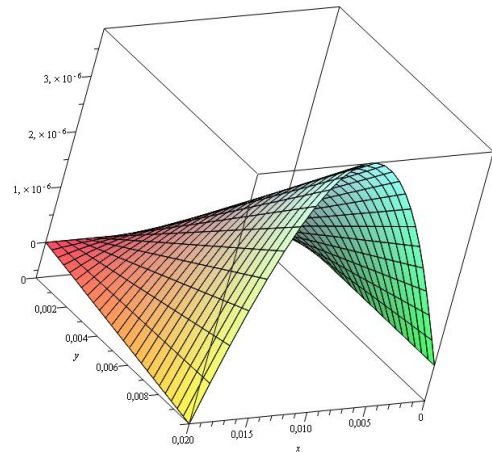


Fig 12. - Simulation of thermal conductivity at  $t=1s$ ,  $z=0.005m$ , at  $x=0...0.02$ ,  $y=0...0.01$

The result of calculating the function  $q$  is a complex polynomial containing trigonometric and exponential components grouped by degrees of variables.

An analysis of the resulting mathematical model (based on the output of the  $q$  function from the Maple environment) shows:

1. Non-linearity of distribution: The presence of terms of the form  $\sin(\frac{\pi x}{20})$  and  $\sin(\frac{\pi y}{10})$  indicates that the heat flow is distributed unevenly. The greatest thermal load is concentrated in the active area of the transistor channel.
2. Time factor: The coefficient  $e^{-t}$  simulates the process of cooling or establishing thermal equilibrium after removing the pulse load. At  $t=10$ , the system demonstrates stabilization of the thermal profile.
3. The influence of materials: varying the parameter  $a$  allows you to adapt the model to new materials. For example, when replacing a silicon substrate with silicon carbide (SiC), the thermal conductivity coefficient will increase significantly, which will be reflected on the graph as a flatter surface without pronounced "thermal peaks".

The program output shows that the peak values of temperature gradients are localized in the central regions of the crystal, where the sine function reaches a maximum, and decrease exponentially to the edges. This computational algorithm can be integrated into the memory subsystems of microcontrollers (where the transistors are located as tightly as possible) for predictive throttling – automatically reducing the frequency of information recording in case of a threat of local overheating.

Comparative analysis showed that when using 4H-SiC (with a calculated coefficient of  $a=0.43$ ), the relaxation rate of thermal energy increases by several orders of magnitude compared to silicon structures ( $a=0.000028$ ).

## Conclusion

The study examined the problem of thermal conductivity in the transistor structures of modern microcontrollers.

1. The evolution of the development of field-effect transistors from the first MOSFET structures to modern solutions based on Trench MOSFET, DirectFET and innovative materials (SiC, GaN) is analyzed. It is revealed that insufficient heat sink is a key obstacle for further miniaturization.
2. Using the Maple 13 computer algebra system, a mathematical model of heat propagation was implemented. The algorithm used to decompose the function into a series of polynomials made it possible to approximate the three-dimensional Fourier equation for the local region of the transistor with high accuracy.
3. The results obtained show how long it takes for heat to be distributed across the stock crystal, and how long it takes for the transistor's heat sink to be effective. The proposed model can serve as an effective CAD tool in designing the topology of Internet of Things microcontrollers.

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