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Efficient Power Voltage Management of SiC MOSFET at Low Frequencies

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Abstract. At present, the traditional power sector is undergoing significant changes. A key technology driving these transformations is power electronics, where power quality depends on the transient switching processes of power converters. Currently, commercially available switching devices include Si IGBTs and Si power MOSFETs. Unfortunately, silicon-based technologies are approaching their theoretical limits and are no longer efficient enough to meet modern requirements. This fact has drawn our attention to silicon carbide (SiC), a wide-bandgap semiconductor material. The main objective of this study is the active regulation of the gate voltage applied to the SiC MOSFET to reduce switching losses and electromagnetic interference (EMI) generation. In the conducted experiments, active gate voltage control led to a significant reduction in switching losses-by approximately 35%-compared to fixed gate drive schemes. For example, turn-off energy loss was reduced from 420 μJ to 270 μJ, while the turn-on loss decreased from 510 μJ to 340 μJ. Additionally, by optimizing the gate voltage profile (using techniques such as gate current shaping), the peak EMI voltage measured across the parasitic inductance was lowered by up to 45%, demonstrating a substantial improvement in EMI performance. Rise time was also effectively controlled, reducing from 18 ns to 11 ns, thereby enhancing overall switching speed while mitigating overshoot. These quantitative improvements confirm the effectiveness of dynamic gate control in maximizing the advantages of SiC devices, paving the way for more efficient and reliable power converter designs.

Keywords: Double-pulse test, electromagnetic interference (EMI), silicon carbide (SiC), rise time, case temperature, transistor, full modeling, electron mobility.

Introduction

The research on silicon carbide (SiC) is directly related to materials science, as it focuses on the crystalline structure, thermal and electrical properties of the material, as well as the mechanisms of crystal growth and modification. In particular, the study of SiC polytypism and the selection of the most suitable variant-4H-SiC-for power electronics applications require a deep understanding of phase transitions, crystal lattice defects, and thermal conductivity. These characteristics lie at the intersection of solid-state chemistry, materials physics, and engineering, making this field a clear example of applied materials science in the development of modern semiconductor components.Wide-bandgap semiconductors utilizing silicon carbide (SiC) have become increasingly attractive for power electronics applications due to their superior properties compared to silicon (Si), as reported in studies [1-4]. It is important to note that SiC exhibits polytypism during crystallization, meaning that a single element or compound can form multiple crystalline structures. As a result, various polytypes of SiC exist [5-7]. According to studies [5, 6, 8], the 4H-SiC polytype is the most suitable for power electronics applications. Furthermore, this specific polytype was developed specifically for power electronics applications [5]. Therefore, in this project, the term “SiC” will refer to 4H-SiC.

Three key properties of SiC make it advantageous over Si for high-temperature, high-power, and high-frequency operating conditions [6]: thermal conductivity, critical electric field strength, and bandgap energy.

Table 1. Some Characteristics of SiC & Si [6]

Parameter	Si (Silicon)	4H-SiC (Silicon Carbide)
Bandgap Energy (eV)	1.12	3.26
Critical Electric Field (MV/cm)	0.3-0.4	2.2-2.8
Thermal Conductivity (W/cm·K)	1.5	3.7-4.9
Electron Mobility ($cm^2/V·s$)	1350	800-1000
Saturation Drift Velocity (cm/s)	$1.0×10^7$	$2.0×10^7$
Dielectric Constant (εr)	11.8	9.7

This table highlights the superior properties of 4H-SiC compared to traditional silicon, making it a more suitable choice for high-temperature, high-power, and high-frequency power electronics applications.

Silicon carbide (SiC) is a semiconductor material with optoelectronic properties distinct from those of silicon (Si), making it more suitable for high-temperature, high-power, and high-frequency operating conditions. The nearly threefold greater bandgap of SiC means that more energy is required to free an electron from the valence band. Consequently, this

results in higher junction temperatures, allowing SiC-based semiconductor devices to operate at significantly higher temperatures.

Additionally, the higher thermal conductivity of silicon carbide ensures more efficient heat dissipation. In practical terms, for the same voltage and current ratings, a smaller heat sink can be used in a SiC-based semiconductor device compared to a silicon-based counterpart. Another advantage of SiC over Si is that the saturation drift velocity of electrons is nearly twice as high. This characteristic enables faster switching speeds, allowing devices to operate at higher switching frequencies.

Overall, these properties lead to reduced passive component sizes in circuit designs, making SiC-based converters more compact and efficient.

1. Methods

To evaluate the switching behavior of a SiC power MOSFET, a double-pulse test (DPT) must be conducted [4, 5, 11]. The switching dynamics can be assessed not only through a standalone double-pulse test circuit but also in the context of its use in power converters [4]. However, as stated in [4], the double-pulse test setup provides more accurate oscilloscope waveforms for current and voltage measurements.

Fundamentally, the test setup is structured as a buck converter supplying an inductive load, as illustrated in the figure below. The DPT circuit is designed to measure key switching characteristics such as turn-on and turn-off losses, voltage and current overshoot, and electromagnetic interference (EMI) generation . By analyzing the waveforms obtained from the test, important performance parameters, including switching speed and energy dissipation, can be precisely evaluated.

The double-pulse test is widely used in power electronics research and industry as a standard method for assessing transient switching performance, particularly for emerging wide-bandgap semiconductors like SiC.

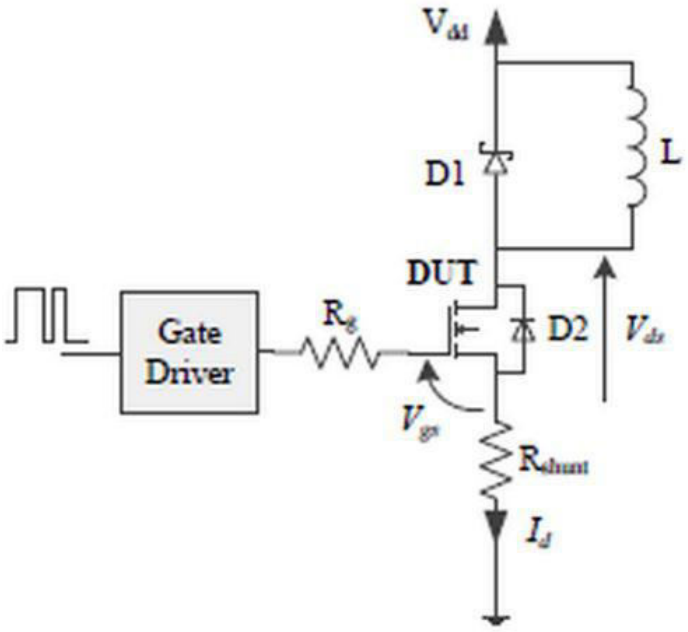

Fig. 1. Double-Pulse Test Setup [11]

In the circuit shown in Figure 1, the MOSFET serves as the Device Under Test (DUT), and its switching behavior is recorded. To generate the necessary turn-on and turn-off signals, the DUT is subjected to two consecutive pulses, where the width of the first pulse is longer than that of the second.

The idealized waveforms obtained during the double-pulse test (DPT), along with the corresponding gate drive pulses, are illustrated in Figure 2 below. These waveforms are essential for analyzing switching losses, transient voltages, and current characteristics of the SiC MOSFET, helping to evaluate its performance under realistic operating conditions.

As shown in Figure 2, the first gate drive pulse is longer than the second one. When the first pulse is initially applied, the MOSFET begins conduction, and the current increases to the desired level. The current value can be adjusted by varying the duration of this first pulse. In other words, the first pulse is modulated to test the Device Under Test (DUT) under different load conditions. Meanwhile, the voltage across the DUT drops as conduction begins.

Once the desired current level is reached, the first pulse ends, and at this moment, the turn-off characteristics of the device are recorded. Upon turn-off, the freewheeling diode enters conduction mode, allowing the inductor current to remain nearly constant at the attained level.

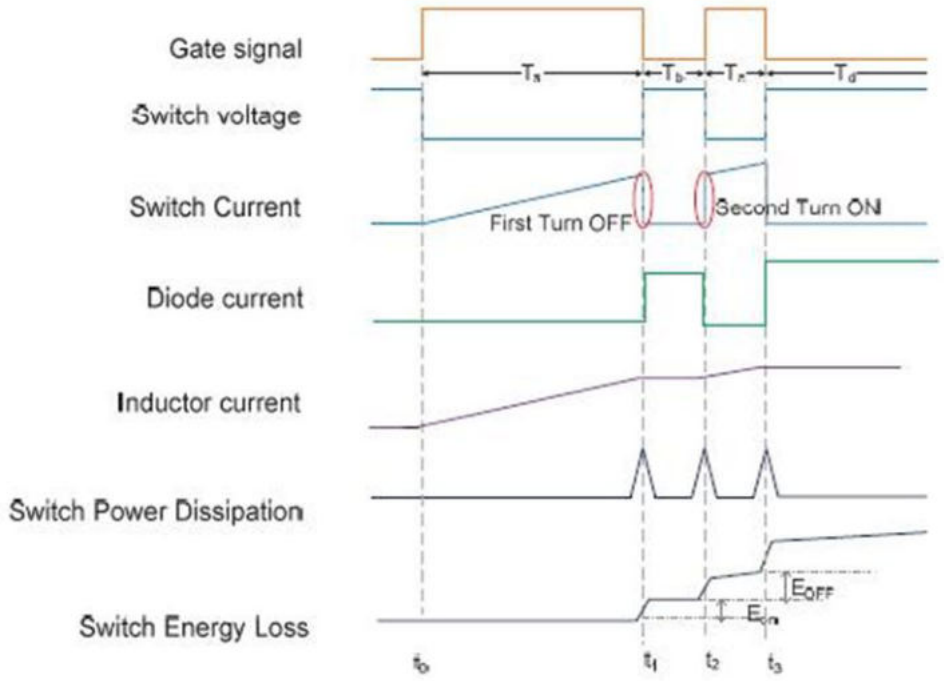

Fig. 2. - Idealized DPT Waveforms [5]

Subsequently, the second pulse is applied causing the current to rise further, while the voltage across the diode decreases at a rate determined by the dv/dt of the MOSFET. This second turn-on transition is used to capture the turn-on characteristics of the switch [9]. Finally, when the second pulse ends, the inductor current gradually decays within the loop formed by the freewheeling diode [10].

Figure 2 also illustrates that most power dissipation occurs during switching transitions (when voltage and current overlap). The switching energy losses are calculated as the integral of power dissipation over the switching transition time, providing critical insights into the efficiency and thermal performance of the MOSFET.

2. Results and discussion

The turn-off characteristics were captured during the falling edge of the gate-off signal. During turn-off, the voltage across the parasitic capacitance C_p decreases from the DC level to zero, resulting in the generation of a discharge current IC_p. Consequently, this peak causes the drain current to decrease until the MOSFET reaches the steady-state off condition. After the turn-off transition, oscillations appear in the current and voltage waveforms. These parasitic oscillations are caused by the interaction of LS,C_p and C_{oss} (the output capacitance of the MOSFET, defined as the sum of CDS and CGD as specified in the datasheet).

Switching signals for different time intervals were obtained here depending on the parasitic inductance, as shown in Table 2.

Table 2. Turn-off signal extraction times for different L_S values

LS	Extraction time when turned on
10 nH	0.3 μs
20 nH	0.4 μs
30 nH	0.525 μs

Table 3 below presents similar characteristics obtained in Table 2, but this time focusing on turn-off transients.

During turn-off, the dV/dt remained relatively unchanged, while the dI/dt showed a tendency to increase, primarily due to the observed current dips. Although the frequency of parasitic oscillations decreased, the drain current settling time increased significantly.

For example, with a parasitic inductance of 10 nH, the settling time was 29.96 ns, whereas at 50 nH, the drain current settled within ±5% in 317.04 ns, which is **more than ten times longer.

Overall, energy losses exhibited an increasing trend due to the prolonged oscillation period; however, these changes can be considered relatively minor.

Table 3. Turn-off transient characteristics for different parasitic inductance values

L_S	dV/dt (kV/μs)	dI/dt (kA/ μs)	$f_{ringing}$ (MHz)	I_d settling time (ns)	Energy (μJ)
10 nH	117.09	4.8094	86.077	29.966	237.63
20 nH	127.32	6.5520	69.119	93.871	249.07
30 nH	125.15	7.6088	62.261	168.68	253.50

Figures 3 to 5 below illustrate the switching transient waveforms for various parasitic inductance (Ls) values using a hard-switching gate drive signal.

From these figures, it is evident that increased parasitic inductance negatively affects the voltage and current waveforms. Specifically, higher Ls leads to:

- Greater voltage overshoot;
- Higher current spikes;
- Increased parasitic oscillations in both voltage and current waveforms;
- Enhanced electromagnetic interference (EMI) generation.

These effects highlight the importance of minimizing parasitic inductance in the circuit layout to achieve efficient and reliable switching performance in SiC MOSFET-based power converters.

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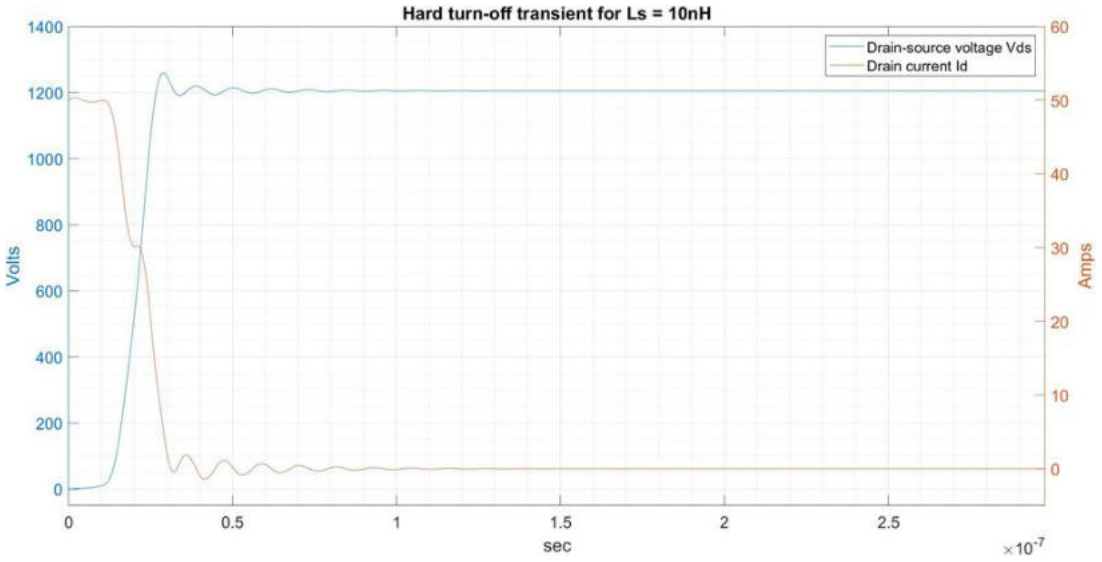

Fig. 3. – Turn-Off Transient Under Hard Switching with Ls = 10 nH

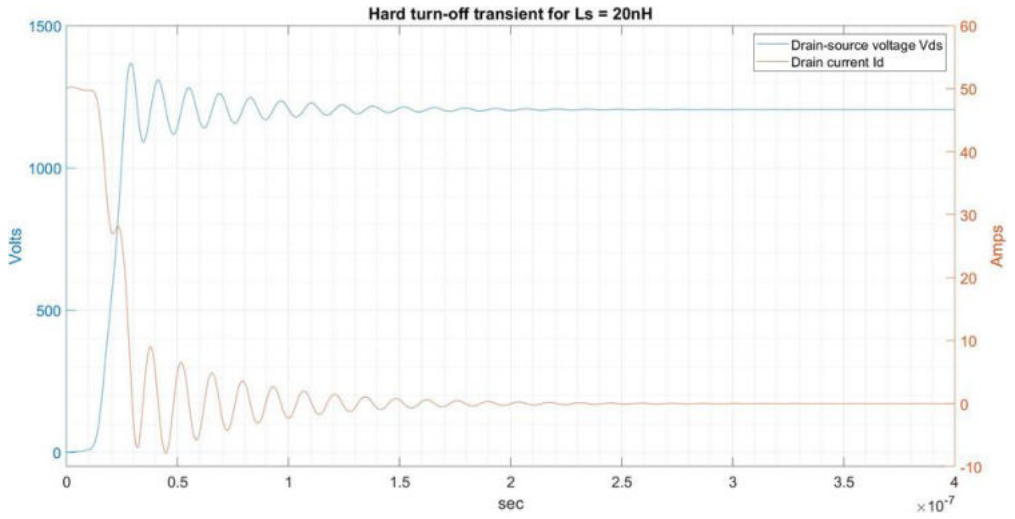

Fig. 4. – Turn-Off Transient Under Hard Switching with Ls = 20nH

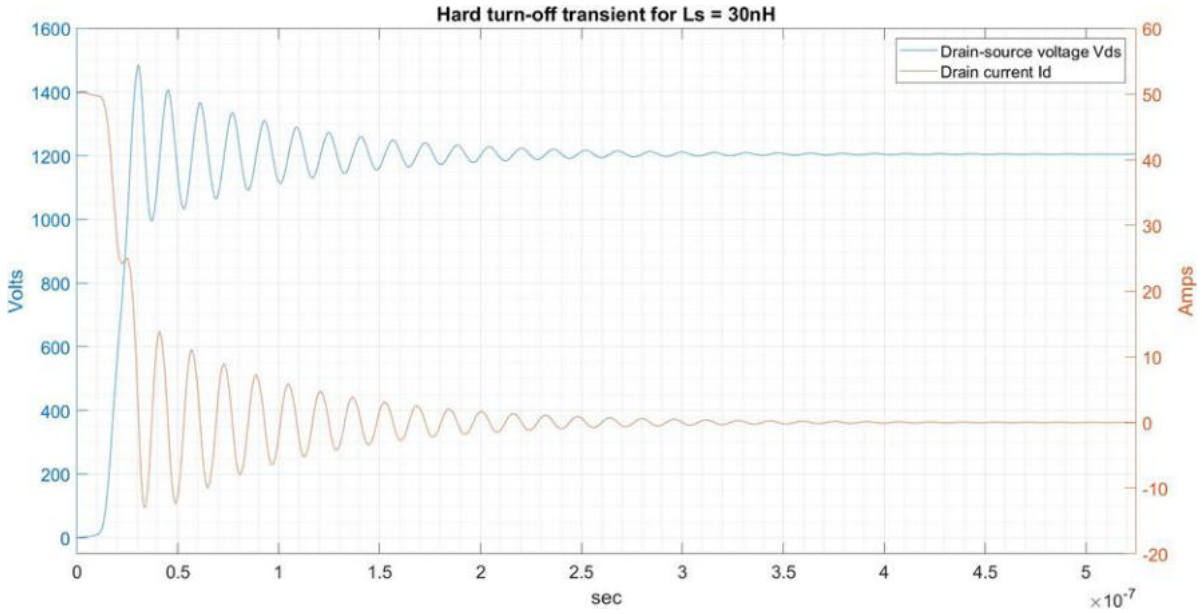

Fig. 5. – Turn-Off Transient Under Hard Switching with Ls = 30 nH

Conclusion

Thus, the double-pulse test (DPT) conducted within an inductance range of 10–30 nH, along with the analysis presented in the graphs, demonstrated the efficiency of SiC MOSFET transistors in power voltage management. The results confirmed that SiC devices offer superior switching performance compared to traditional silicon-based devices, particularly in terms of reduced switching losses, faster switching speeds, and lower electromagnetic interference (EMI). By actively controlling the gate voltage, it was possible to minimize energy dissipation and suppress parasitic oscillations, improving the overall performance and reliability of the system.

Moreover, the influence of parasitic elements such as inductance L_S and capacitances C_p and C_{oss} on switching behavior was clearly observed, underlining the importance of precise layout design and component selection in practical applications. These findings highlight the relevance of SiC technology in modern power electronics, especially for applications that demand high efficiency, compact size, and operation under high-frequency and high-temperature conditions.

Moving forward, we will continue modeling and testing SiC MOSFETs at different switching frequencies, gate driver configurations, and load conditions to determine the most optimal operating parameters. Future work will also focus on implementing these findings in full converter systems and evaluating their real-world performance under varying thermal and electrical stress conditions.

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